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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yasushi KOUBUCHI, ET AL.

Serial No.: Rule 1.53(b) continuation of U.S. Patent Application Serial No.: 10/075,246, filed February 15, 2002

Filed: July 14, 2003

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND FABRICATION PROCESS AND DESIGNING METHOD THEREOF

Group of parent: 2825

Examiner of parent: Lee

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 30, 2003

Sir:

Pursuant to the requirements of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on

(1) Japanese Patent Application No. 09-081013, filed in Japan on March 31, 1997; and

(2) Japanese Patent Application No. 10-033388, filed in Japan on February 16, 1998.

Certified copies of the above-listed Japanese Patent Applications were submitted in prior application Serial No. 09/050,416, filed March 31, 1998, on April 24, 1998.

Respectfully submitted,

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